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Harmonic Minimization in 31-Level Cascaded Multilevel Inverter Topology with Reduced Number of Switches

Koyyana Srinivasa Rao[1], K.Nagamani[2], Dhanunjaya Naidu[3]
[1]*Asst.professor, Dept. of EEE, Lendi institute of engineering and technology, AP, India*
[2]*Asst.professor, Dept. of EEE, Lendi institute of engineering and technology, AP, India*
[3]*Asst.professor, Dept. of EEE, Lendi institute of engineering and technology, AP, India*
Corresponding Author: Koyyana Srinivasa Rao

Abstract: *Multilevel inverters are power electronic devices that changes over DC to AC quantity. But these devices produces non-sinusoidal signal which contains harmonics. So as to be overcome this problem a 31-level cascaded multilevel inverter topology was developed. The proposed inverter topology has been designed based on the minimum number of switches, switching power losses and total harmonic distortion[THD] when compared to the symmetrical seven level and asymmetrical fifteen level inverter topology. The simulation results are presented showing the validity of the analysis.*
Index terms: multilevel inverter, power electronics, fundamental switches

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I. Introduction

Multilevel power conversion was first introduced more than twenty years ago. The multilevel inverter has drawn tremendous interest in the power in the power industry. They present a new set of features that are well suited for use in reactive power compensation. By using multilevel inverter to produce quality output voltage or a current waveform with minimum amount of ripple content. It can be possible by using more number of active semiconductor switches to perform conversion in small voltages steps. There are several advantages in process when compare to the conventional power conversion approach. One area where multilevel converters are mostly suitable is that of renewable photovoltaic energy that efficiency and power quality are of concerns for the researchers. Multilevel inverter mostly popular area where the numbers of switches are reduced.

This paper discusses the operation of different topologies for multilevel inverter which can produce multilevel. The multilevel inverter concept is the kind of alternation of two-level inverter. The general structure consists of four switches found in the single phase inverter is to create a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The main motivation for such inverter is that the current is shared among these multiple switches, allowing a high inverter power rating than the individual switch VA rating. Otherwise it allows harmonics. As the number of level increase, the synthesized output waveform.

Several types of multilevel inverter topologies, which have been reported from high power inverter system manufactures. The most commonly used topologies are diode clamped, flying capacitor, cascaded H-Bridge and modified H-bridge multilevel inverter topologies. These three topologies employ different mechanism to produce the required output. But requirement switches are more and power loss also more. For example symmetrical seven level multilevel inverter require 10 switches.

II. Cascaded multilevel inverter

A cascaded multilevel inverter has of number of H-bridge inverter units associated in series and they are sustained from discrete DC sources. As they yield is taken in series, the DC sources must be isolate from each other. Therefore, cascaded multilevel inverter is additional been proposed to be utilized with energy components or photovoltaic clusters keeping in mind the goal to accomplish higher voltage level. The subsequent AC yield voltage is the expansion of the voltages produced by various H- bridge cells. Each bridge has the property to create three levels as $+V_{dc,}$ 0, $-V_{dc}$ by associating the DC source to the AC yield and by various mixes of four switches where V_{dc} is the input voltages of the H- bridge.

2.1 Seven level multilevel inverter topology

A seven level multilevel inverter block diagram as shown in below

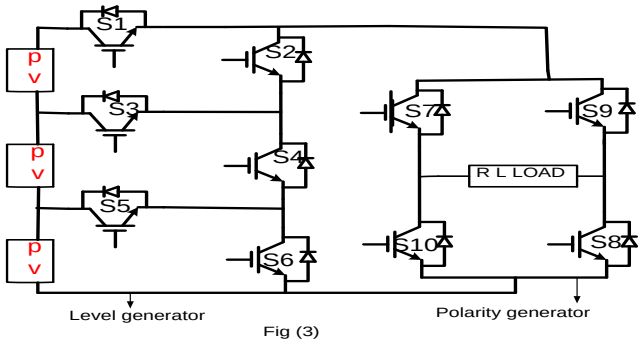

Fig1. Seven level multilevel inverter topology

State 1:

The switches S_2 S_4 S_6 S_7 S_8 are ON and remaining switches are OFF then short circuit across the output terminals. So zero output voltage is generated.

State 2:

The switches S_2 S_4 S_5 S_7 S_8 are ON and remaining switches are OFF then 1Pu will be appearing across the output terminals.

State 3:

The switches S_2 S_3 S_7 S_8 are ON and remaining switches are OFF then 2Pu will be appearing across the output terminals.

State 4:

The switches S_1 S_7 S_8 are ON and remaining switches are OFF then peak 3Pu will be appearing across the output terminals.

Multilevel PWM technique:

In multilevel PWM modulation technique used three reference signals those are $V_{ref1,}V_{ref2,}V_{ref3}$ and one carrier signal $V_{cr.}$ Reference signals have the same frequency equal to the line frequency and the same amplitude. They are in phase with each other with the offset value equal to the amplitude of carrier signal. There are three reference signal compare to the carrier signal. . If V_{ref1} take turn when it exceeds the peak of carrier signal V_{cr}. And the V_{ref2} take turn when it exceeds the peak of carrier signal V_{cr}. And V_{ref3} take turn when it exceeds the peak of carrier signal V_{cr} until it reaches to zero. One V_{ref3} reaches zero ,V_{ref2} will be compared again until it reaches zero. Onwards V_{ref1} will be compared with carrier V_{cr}.

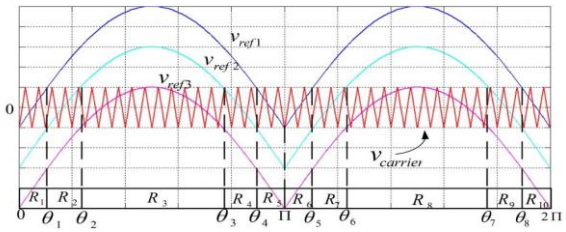

Fig2. PWM technique

States are determined as follows

State1: $\mathbf{0} < \omega t < \theta 1$ and $\theta 4 < \omega t < \pi$

State2: $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$

State3: $\theta 2 < \omega t < \theta 3$

Phase angle displacement cab be determined from above fig4.we can observe that at $\theta 1$ reference signal and carrier signal are equal. Carrier signal magnitude V_{cr} and reference signal magnitude $V_m \sin \theta 1$. Mathematically can be explained as in below

$V_{cr} = V_m \sin \theta 1$ there fore $\theta 1 = \sin^{-1}(\text{Vcr}|\text{Vm})$ and same as $\theta 5$.

$$\theta 2 = \theta 6 = \sin^{-1}(\text{Vcr}|\text{Vm})$$
$$\theta 3 = \pi - \theta 2$$
$$\theta 4 = \pi - \theta 1$$
$$\theta 7 = 2\pi - \theta 6$$
$$\theta 8 = 2\pi - \theta 5$$

Modulation index can be determined by using in this inverter. Modulation index can be defined as the ratio of amplitude of reference signal to amplitude of carrier signal

M_a=(Vm|3Vcr)

V_m = amplitude of reference signal

V_{cr} = amplitude of carrier signal

In this proposed topology modulation index can be determined as 0.9.

Switching functions:

$S_1 = C_3 * R_3$

$S_2 = \bar{S}_1$

$S_3 = C_2*[R_2+R_4]+\bar{C}_3*R_3$

$S_4 = \bar{C}_2*[R_1+R_2+R_4+R_5]$

$S_5 = C_1*[R_1+R_5]+\bar{C}_2*[R_2+R_4]$

$S_6 = \bar{C}_1*[R_1+R5]$

S_7 and S_8 are ON during positive polarity output. S_9 and S_{10} are ON during negative polarity output. From above switching functions where '+' represent as logical OR gate. '*' represent as logical AND gate. '−'Represent as logical inverse [NOT].The efficiency of inverter depends up on the number of switching are conducting. Because the numbers of switches are conducting stage are more then the switching losses are more so efficiency are less. In this proposed topology conducting switches lower than the cascaded inverter. So efficiency will be improved.

2.1 Fifteen level multilevel inverter topology

A fifteen level multilevel inverter block diagram as shown in figure.

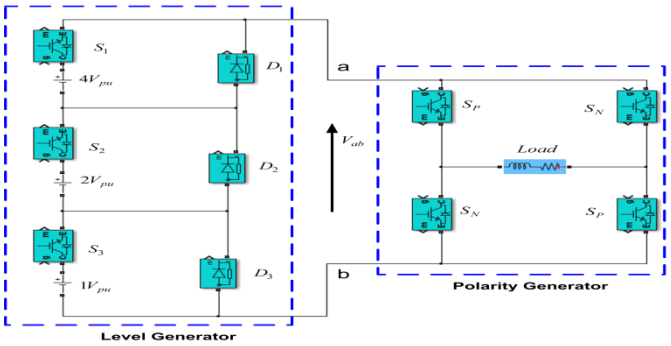

Fig3. Fifteen level multilevel inverter topology

State 1:

V_{ab} = 0Pu To obtain this state of level 0 all the switches are turned OFF.

State 2:

V_{ab} = 1Pu To obtain this state of level switches S_3, S_p are ON and remaining switches are OFF.

State 3:

V_{ab} = 2Pu To obtain this state of level switches S_2, S_p are ON and remaining switches are OFF.

State 4:

V_{ab} = 3Pu To obtain this state of level switches S_3, S_2, S_p are ON and remaining switches are OFF.

State 5:

V_{ab} = 4Pu To obtain this state of level switches S_1, S_p are ON and remaining switches are OFF.

State 6:

V_{ab} = 5Pu To obtain this state of level switches S_1, S_3, S_p are ON and remaining switches are OFF.

State 7:

V_{ab} = 6Pu To obtain this state of level switches S_1, S_2, S_p are ON and remaining switches are OFF.

State 8:

V_{ab} = 7Pu To obtain this state of level switches S_1, S_2, S_3, S_p are ON and remaining switches are OFF.

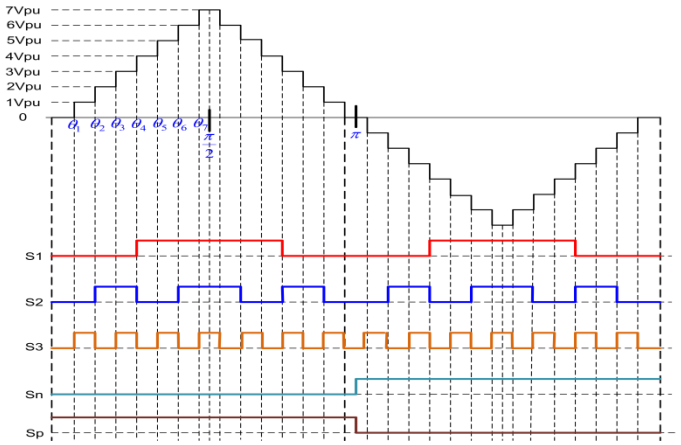

Fig4. Stepped-voltage waveform consists of the output of proposed inverter topology.

Fig. 4 shows the Stepped-voltage waveform consists of the output of proposed inverter with switching angles for 10 IGBTs. According to the operating states and the output voltage level to be generated the gate pulses for all the switches are derived.

III. Proposed Topology

The proposed topology has ten power electronics switches with four DC sources as shown in fig below. The power electronics switches are denoted with normal switches. But in practical application either IGBT'S or MOSFET'S are used for the switching operation.

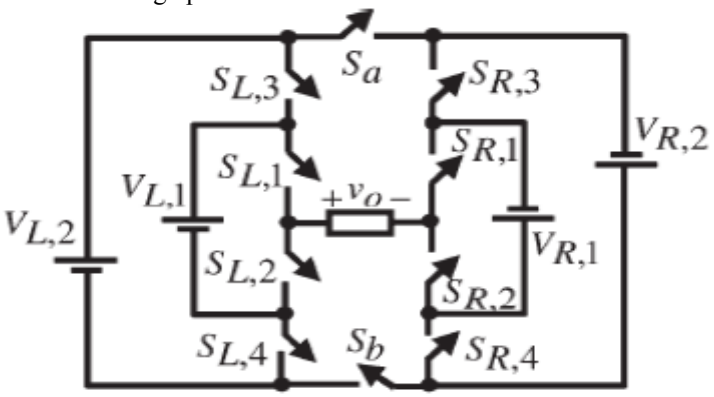

Fig5. Proposed 31-level inverter topology

The switching operation of 31-level multilevel inverter can be shown in below table. The magnitude of DC sources of the proposed 31-level inverter are recommended as follows

$$V_{L1}=V_{DC}$$
$$V_{R1}=2V_{DC}$$
$$V_{L2}=5V_{DC}$$
$$V_{R2}=10V_{DC}$$

The proposed topology are obtained by adding two unidirectional power switches and one dc voltage sources to the H-bridge inverter structure. In proposed topology there six unidirectional switches (S_a , S_b ,$S_{L1,}$ $S_{L2,}$ S_{R1} and S_{R2}) .

S.NO	S_{L1}	S_{L2}	S_{L3}	S_{L4}	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_a	S_b	Output voltage(V_0)
1	1	0	1	0	1	0	1	0	1	0	0
	0	1	0	1	0	1	0	1	0	1	0
2	0	1	0	1	1	0	0	1	0	1	V_{L1}
3	1	0	0	1	0	1	0	1	0	1	V_{R1}
4	1	0	0	1	1	0	0	1	0	1	$V_{L1}+ V_{R1}$
5	0	1	0	1	0	1	1	0	0	1	$V_{L2}-V_{L1}$
6	0	1	0	1	1	0	1	0	0	1	V_{L2}
7	1	0	0	1	0	1	1	0	0	1	$V_{L2}+ V_{R1}- V_{L1}$
8	1	0	0	1	1	0	1	0	0	1	$V_{L2}+ V_{R1}$
9	0	1	1	0	0	1	0	1	0	1	$V_{R2}- V_{R1}$
10	0	1	1	0	1	0	0	1	0	1	$V_{L1}- V_{R1}+ V_{R2}$
11	1	0	1	0	0	1	0	1	0	1	V_{R2}

12	1	0	1	0	1	0	0	1	0	1	$V_{L1}+ V_{R2}$
13	0	1	1	0	0	1	1	0	0	1	$V_{L2}+ V_{R2}- V_{L1}- V_{R1}$
14	0	1	1	0	1	0	1	0	0	1	$V_{R2}+ V_{L2}- V_{R1}$
15	1	0	1	0	0	1	1	0	0	1	$V_{L2}+ V_{R2}- V_{L1}$
16	1	0	1	0	1	0	1	0	0	1	$V_{L2}+ V_{R2}$
17	0	1	0	1	0	1	0	1	1	0	$-(V_{L2}+ V_{R2})$
18	0	1	0	1	1	0	0	1	1	0	$-(V_{L2}+ V_{R2}- V_{L1})$
19	1	0	0	1	0	1	0	1	1	0	$-(V_{R2}+ V_{L2}- V_{R1})$
20	1	0	0	1	1	0	0	1	1	0	$-(V_{L2}+ V_{R2}- V_{L1}- V_{R1})$
21	0	1	0	1	0	1	1	0	1	0	$-(V_{L1}+ V_{R2})$
22	0	1	0	1	1	0	1	0	1	0	$-(V_{R2})$
23	1	0	0	1	0	1	1	0	1	0	$-(V_{L1}- V_{R1}+ V_{R2})$
24	1	0	0	1	1	0	1	0	1	0	$-(V_{R2}- V_{R1})$
25	0	1	1	0	0	1	0	1	1	0	$-(V_{L2}+ V_{R1})$
26	0	1	1	0	1	0	0	1	1	0	$-(V_{L2}+ V_{R1}- V_{L1})$
27	1	0	1	0	0	1	0	1	1	0	$-(V_{L2})$
28	1	0	1	0	1	0	0	1	1	0	$-(V_{L2}-V_{L1})$
29	0	1	1	0	0	1	1	0	1	0	$-(V_{L1}+ V_{R1})$
30	0	1	1	0	1	0	1	0	1	0	$-(V_{R1})$
31	1	0	1	0	0	1	1	0	1	0	$-(V_{L1})$

Table1.switching operation of 31 level inverter topology

From the above table 1 and 0 indicate the ON and OFF states of the switches respectively. The 31-level inverter topology the magnitude of V_{L1} and V_{R1} should be considered 1pu and 2pu respectively and also V_{L2} and V_{R2} should be 5pu and 10pu. Considering the after mentioned explanations the total number of switches and cost of proposed topology is low because DC voltage sources with low magnitude are needed.

3.1 comparison of components required for proposed topology with other popular inverters

Components	Symmetrical 7- level inverter	Asymmetrical 15- level inverter	Proposed multi level inverter topology
Main switches	12	12	10
Main diodes	12	12	10
Dc sources	3	3	4
Total components	27	27	24

Table2. Comparison of different inverter topology

IV. Simulation Results

In order to verify the correct performance of the proposed multilevel inverter is generating all output voltage levels(even and odd). The simulation diagram of 31-level inverter as shown in below.

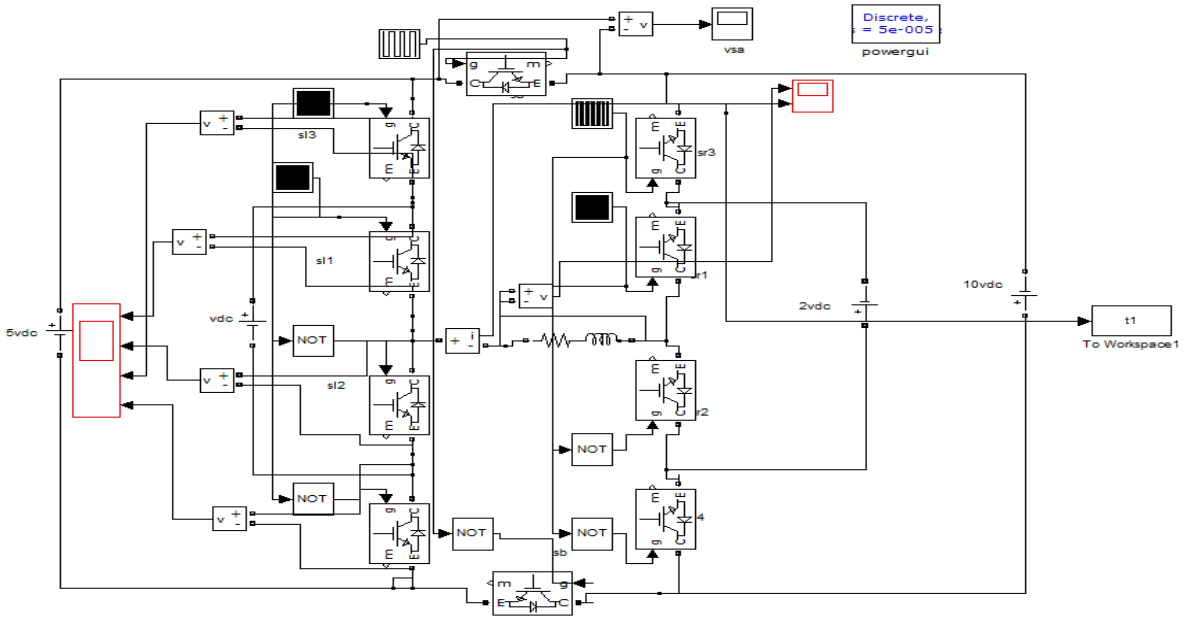

Fig6. Simulation diagram of 31-level inverter

The output waveforms of the inverter feeding resistance and inductance as shown in below

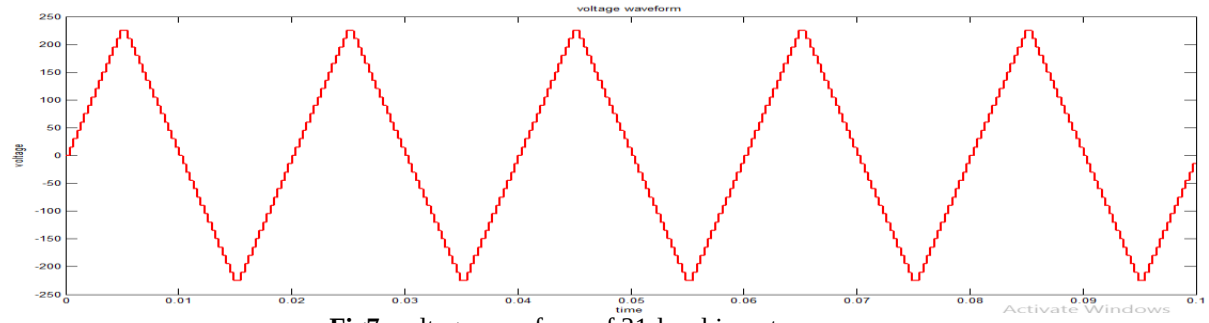

Fig7. voltage waveform of 31-level inverter

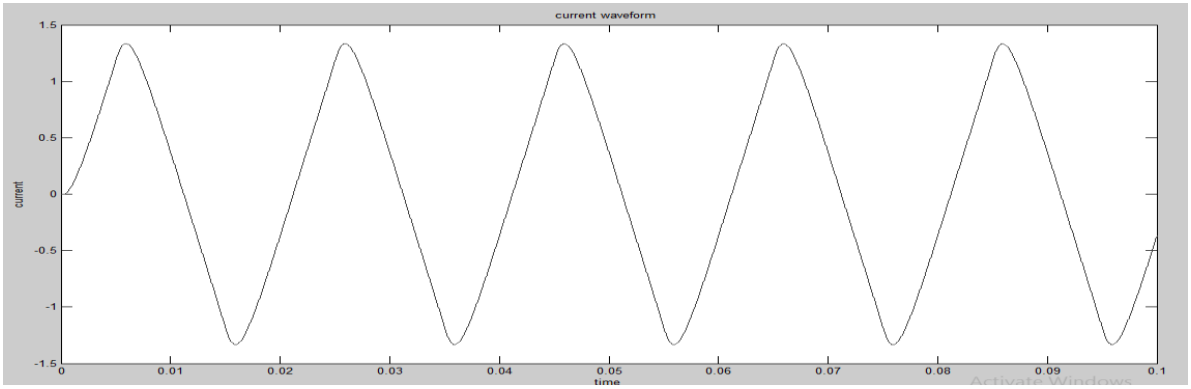

Fig8. current waveform of 31-level inverter

The %THD of current waveform is 9.16% without filter as shown in below

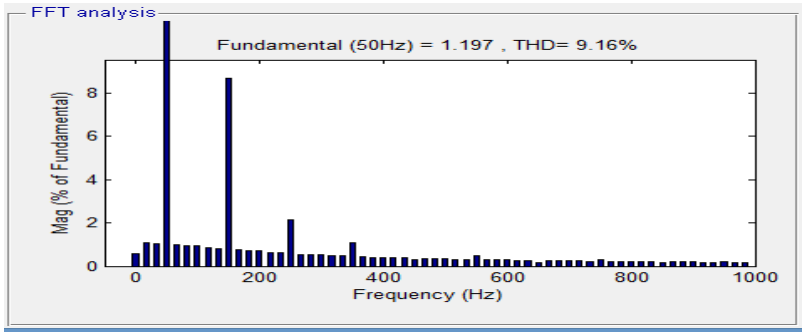

Fig9. current waveform THD for 31-level inverter

The output waveforms of the7-level inverter feeding resistance and inductance as shown in below

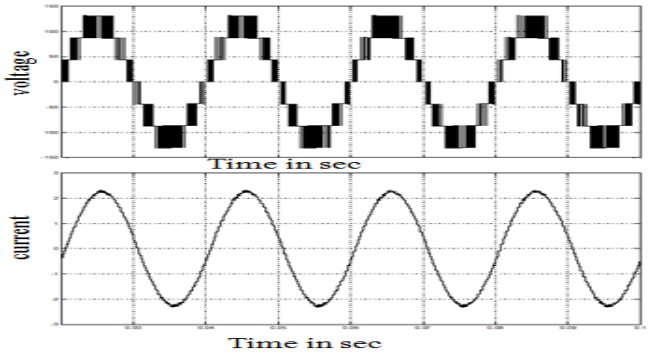

Fig10. Voltage and current waveform of 7-level inverter

The output waveforms of the15-level inverter feeding resistance and inductance as shown in below

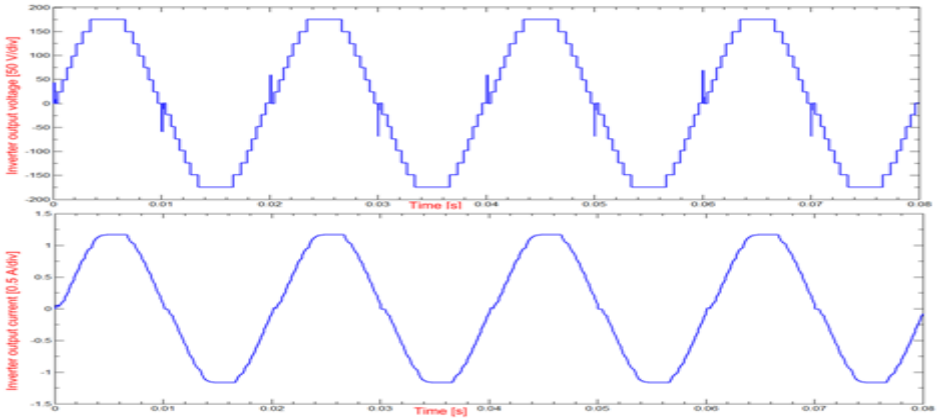

Fig11. Voltage and current waveform of 15-level inverter

V. Conclusion

In this paper 31-level multilevel inverter topology performs good and produced output voltage near to sine wave and lower THD value without using filtering. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison results, the proposed

Topology requires a lesser number of IGBTs, power diodes, and dc voltage sources Cost and control system are more reliable.

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AUTHORS DETAILS

Mr.Koyyana Srinivasa Rao received the B.Tech Degree in Electrical & Electronics Engineering from T.P.I.S.T, Bobbili, Vizianagaram, India in 2012 and M. Tech in Aditya Institute of Technology & Management, Tekkali, Srikakulam, India in 2015. He has 3 years of Experience, Currently he is working as asst.professor in the Department of Electrical & Electronics Engineering, lendi institute of engineering and technology, vizianagaram dist,andhrapradesh. His research interest, Power electronics and Drives.

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